CLAIMS

Having thus described my invention in detail, what I claim is new, and desire to secure by the Letters Patent is:

1. A method of providing a substantially planar trench isolation region having rounded trench isolation/substrate corners, said method comprising the steps of:

(a) forming a film stack on a surface of a substrate, said film stack comprising an oxide layer, a polysilicon layer and a nitride layer;

(b) patterning said film stack so as to form at least one trench within said substrate, wherein said patterning exposes sidewalls of said oxide layer, polysilicon layer and nitride layer;

(c) oxidizing the at least one trench and said exposed sidewalls of said oxide layer and said polysilicon layer so as to thermally grow a conformal oxide layer in said trench and on said exposed sidewalls of said oxide layer and said polysilicon layer;

(d) filling said trench with a trench dielectric material; and

(e) planarizing to said surface of said substrate.

2. The method of Claim 1 wherein said substrate is composed of Si, Ge, SiGe, GaAs, InAs, InP or a layered semiconductor.

3. The method of Claim 1 wherein said oxide layer of said film stack is thermally grown or deposited.

4. The method of Claim 3 wherein said oxide layer of said film stack is deposited by chemical vapor deposition (CVD), plasma-assisted CVD, sputtering or evaporation.

5. The method of Claim 1 wherein said oxide layer of said film stack has a thickness of from about 5 to about 20 nm.

6. The method of Claim 5 wherein said oxide layer of said film stack has a thickness of from about 6 to about 12 nm.

7. The method of Claim 1 wherein said polysilicon layer of said film stack is formed by a deposition process selected from the group consisting of CVD, plasma-assisted CVD and sputtering.

8. The method of Claim 1 wherein said polysilicon layer of said film stack has a thickness of from about 25 to about 200 nm.

9. The method of Claim 8 wherein said polysilicon layer of said film stack has a thickness of from about 80 to about 120 nm.

10. The method of Claim 1 wherein said nitride layer of said film stack is formed by a deposition process selected from the group consisting of CVD, plasma-assisted CVD, evaporation and sputtering.

11. The method of Claim 1 wherein said nitride layer of said film stack has a thickness of from about 50 to about 30 nm.

12. The method of Claim 11 wherein said nitride layer of said film stack has a thickness of from about 100 to about 200 nm.

13. The method of Claim 1 wherein said patterning includes lithography and etching.

14. The method of Claim 13 wherein said lithography step includes applying a photoresist to said nitride layer of said film stack, patterning the photoresist by exposure, and developing the pattern in said photoresist.

15. The method of Claim 13 wherein said etching step includes a dry etching process selected from the group consisting of reactive-ion etching (RIE), ion-beam etching, plasma etching or any combination thereof.

16. The method of Claim 1 wherein said oxidizing is carried out in an oxygen-containing atmosphere at a temperature of about 800°C or above and for a time period of about 30 minutes or less.

17. The method of Claim 16 wherein said oxidizing is carried out at a temperature of from about 900° to about 1000°C for a time period of from about 5 to about 10 minutes.

18. The method of Claim 16 wherein said oxygen-containing atmosphere comprises O_2, ozone, N_2O or mixtures thereof.

19. The method of Claim 16 wherein said oxygen-containing atmosphere is admixed with an inert gas, said inert gas being present in an amount of about 90% or less in said mixture.

20. The method of Claim 1 wherein said thermally grown oxide layer has a thickness of from about 10 to about 30 nm.

21. The method of Claim 20 wherein said thermally grown oxide layer has a thickness of from about 18 to about 24 nm.

22. The method of Claim 1 wherein said filling comprising a deposition process selected from the group consisting of CVD, plasma-assisted CVD and sputtering.

23. The method of Claim 1 wherein said trench dielectric material is tetraethylorthosilicate (TEOS), SiO_2 or a flowable oxide.

24. The method of Claim 23 wherein said trench dielectric material is TEOS and a densification step is employed prior to said planarizing.

25. The method of Claim 1 wherein said planarizing comprises chemical-mechanical polishing or grinding.

26. The method of Claim 1 wherein said at least one trench is a deep trench, a moderate trench, a shallow trench or any combinations thereof.

27. The method of Claim 26 wherein said at least one trench is a shallow trench.

28. A semiconductor device comprising at least one substantially planarized trench isolation region formed within a substrate electrically isolating adjacent active devices regions from each other, said planarized trench isolation region containing rounded corners between the top surfaces of the trench isolation region and the substrate.

29. The semiconductor device of Claim 28 wherein said substrate is composed of Si, Ge, SiGe, GaAs, InAs, InP or a layered semiconductor.

30. The semiconductor device of Claim 28 wherein said at least one planarized trench isolation region comprises a deep trench isolation region, a moderate trench isolation region, a shallow trench isolation region or any combinations thereof.

31. The semiconductor device of Claim 30 wherein said at least one planarized trench isolation region is a shallow trench isolation region.

32. The semiconductor device of Claim 28 wherein said at least one planarized trench isolation region includes a thermally grown oxide liner and a trench dielectric material.

33. The semiconductor device of Claim 32 wherein said trench dielectric material is tetraethylorthosilicate (TEOS), SiO_2 or a flowable oxide.